CLAIMS

What is claimed is:

1. A composition, comprising:

   a) passivated semiconductor nanoparticles; and at least one of:

   b) a first cyclic Group IVA compound of the formula (1):

   $$(AH_x)_n, \quad (1)$$

   where n is from 3 to 12, each of the n instances of x is independently 1 or 2, and each A in the formula (1) is independently Si or Ge; and

   c) a second cyclic Group IVA compound of the formula (2):

   $$(AH_x)_m(AH_yR_{z-y})_p(ZR'_w)_q, \quad (2)$$

   where $(m + p + q)$ is from 3 to 12, each of the m instances of x is independently 0, 1 or 2, each of the p instances of y is independently 0, 1 or 2, each of the p instances of z is independently 0, 1 or 2, each of the p instances of $(y + z)$ is independently 1 or 2, each of the q instances of w is independently 0 or 1, at least one of p and q is at least 1, each A in the formula (2) is independently Si or Ge, each R in the formula (2) is independently alkyl, aryl, aralkyl, a halogen, $BH_sR"_{2-s}$, $PH_sR"_{2-s}$, $AsH_sR"_{2-s}$ or $AH_tR"_{3-t}$, where s is 0 to 2, t is 0 to 3, and R" is alkyl, aryl, aralkyl, a halogen, or AH_3, Z is selected from the group consisting of B, P and As, and R' is R or H.

2. The composition of Claim 1, wherein said passivated semiconductor nanoparticles comprise silicon nanoparticles and a passivation layer thereon.

3. The composition of Claim 2, wherein said passivation layer comprises at least one member selected from the group consisting of an alcohol, an alcoholate, a thiol and a thiolate.

4. The composition of Claim 2, wherein said passivation layer comprises an alkyl and/or aralkyl group.

5. The composition of Claim 2, wherein said passivation layer comprises hydrogen and/or halogen atoms.

6. The composition of Claim 5, wherein said passivation layer further comprises a surfactant.

7. The composition of Claim 1, wherein said passivated semiconductor nanoparticles have an average particle diameter of less than 5 nm.

8. The composition of Claim 2, wherein said passivated semiconductor nanoparticles have a particle size distribution of from 0.2 nm to less than 10 nm.

9. The composition of Claim 1, wherein each x in the formula (1) is 2.

10. The composition of Claim 1, wherein each x in the formula (2) is 2.

11. The composition of Claim 1, comprising the first cyclic Group IVA compound of the formula (1) and the second cyclic Group IVA compound of the formula (2).

12. The composition of Claim 1, wherein each A in the formula (1) is Si.

13. The composition of Claim 1, wherein each A in the formula (2) is Si.

14. The composition of Claim 12, wherein n is 5 or 6.

15. The composition of Claim 14, wherein n is 5.

16. The composition of Claim 13, wherein (m + p + q) is 5 or 6.

17. The composition of Claim 16, wherein p is 1 and q is 0.

18. The composition of Claim 17, wherein R is $AH_tR'_{3-t}$.

19. The composition of Claim 18, wherein t is 3.

20. The composition of Claim 11, consisting essentially of said passivated semiconductor nanoparticles and said first and second cyclic Group IVA compounds.

21. The composition of Claim 13, wherein at least one of R and R' in the formula (2) is alkyl, aryl, or aralkyl.

22. The composition of Claim 13, wherein q is at least 1.

23. The composition of Claim 1, further comprising a compound of the formula $(ZH_uR_{3-u})_k$, where Z is selected from the group consisting of B, P and As, u is an integer of from 0 to 3, k is 1 or 2, and R is the same as for the second cyclic Group IVA compound.

24. The composition of Claim 23, wherein R in the formula $(ZH_uR_{3-u})_k$ is H or AH_3, where A is the same as for the second cyclic Group IVA compound.

25. The composition of Claim 23, wherein u is 0 or 3.

26. An ink for making a semiconductor film, comprising:

a) the composition of Claim 1; and

b) a solvent in which said composition is soluble.

27. The ink of Claim 26, wherein said passivated semiconductor nanoparticles, and said at least one of said first cyclic Group IVA compound and said second cyclic Group IVA compound are present in said ink in a percentage by weight of from 0.1% to 50%.

28. The ink of Claim 26, wherein said solvent is aprotic.

29. The ink of Claim 26, wherein said solvent is apolar.

30. The ink of Claim 28, wherein said solvent has a boiling point of less than 250 °C. at atmospheric pressure.

31. The ink of Claim 30, wherein said solvent has a boiling point of less than 150 °C. at atmospheric pressure.

32. The ink of Claim 26, wherein said solvent is selected from the group consisting of alkanes, alkenes, halogenated alkanes, halogenated alkenes, arenes, substituted arenes, ethers, cyclic ethers, aliphatic esters, aliphatic amides and aliphatic sulfoxides.

33. The ink of Claim 26, further comprising one or more additives selected from the group consisting of a tension reducing agent, a surfactant, a thickening agent, and a binder.

34. The ink of Claim 26, consisting essentially of said composition and said solvent.

35. The ink of Claim 26, wherein said passivated semiconductor nanoparticles comprise silicon nanoparticles and a passivation layer thereon.

36. The ink of Claim 26, wherein each A in the formula (1) is Si.

37. The ink of Claim 26, wherein each A in the formula (2) is Si.

38. The ink of Claim 36, wherein n is 5 or 6.

39. The ink of Claim 37, wherein (m + p + q) is 5 or 6, p is 1 and q is 0.

40. The ink of Claim 39, wherein R is AH_3.

41. A method of making a patterned semiconductor film, comprising the steps of:

a) printing a composition comprising a first cyclic Group IVA compound of the formula (1):

$$(AH_x)_n, \quad (1)$$

where n is from 3 to 8 and each A in the formula is independently Si or Ge, and/or a second cyclic Group IVA compound of the formula (2):

$$(AH_x)_m(AH_yR_{z-y})_p(ZR')_q, \quad (2)$$

where (m + p + q) is from 3 to 12, each of the m instances of x is independently 0, 1 or 2, each of the p instances of y is independently 0, 1 or 2, each of the p instances of z is independently 0, 1 or 2, each of the p instances of (y + z) is independently 1 or 2, each of the q instances of w is independently 0 or 1, at least one of p and q is at least 1, each A in the formula (2) is independently Si or Ge, Z is selected from the group consisting of B, P and As, R' is R or H, and each R in the formula (2) is independently alkyl, aryl, aralkyl, a halogen, $BH_sR"_{2-s}$, $PH_sR"_{2-s}$, $AsH_sR"_{2-s}$ or $AH_tR"_{3-t}$, where s is 0 to 2, t is 0 to 3, and R" is alkyl, aryl, aralkyl, a halogen, or AH_3, in a pattern on a substrate; and

b) curing said composition to form said patterned semiconductor film.

42. The method of Claim 41, wherein said composition further comprises semiconductor nanoparticles.

43. The method of Claim 42, wherein said semiconductor nanoparticles comprise passivated semiconductor nanoparticles.

44. The method of Claim 42, wherein said semiconductor nanoparticles comprise silicon nanoparticles.

45. The method of Claim 41, wherein said composition comprises both of said first and second cyclic Group IVA compounds.

46. The method of Claim 41, wherein said curing step comprises sintering said composition to form said patterned semiconductor film.

47. The method of Claim 41, wherein said curing step comprises irradiating said composition to form said patterned semiconductor film.

48. The method of Claim 41, wherein said printing step comprises (i) depositing a layer of said composition on said substrate, and (ii) embossing said layer.

49. The method of Claim 48, wherein said substrate comprises a two-dimensional array of fields, and said embossing comprises contacting a stamp having patterned features therein corresponding to said pattern with said layer in one or more first fields on said substrate, then repeating said contacting step in one or more second fields on said substrate, said second fields being distinct from said first fields.

50. The method of Claim 48, wherein said depositing comprises spin coating, dip coating, or spray coating a solution, emulsion or suspension of said composition on said substrate.

51. The method of Claim 41, wherein said printing step comprises the substeps of depositing a layer of said composition on said substrate, selectively irradiating portions of said layer, and removing either irradiated or non-irradiated portions of said layer to form said pattern.

52. The method of Claim 51, wherein said depositing substep comprises spin coating, dip coating, or spray coating a solution, emulsion or suspension of said composition on said substrate.

53. The method of Claim 51, wherein said selectively irradiating substep comprises (i) positioning at least one of said substrate and a mask such that said portions can be selectively irradiated and said non-irradiated portions cannot be irradiated, and (ii) irradiating said layer with ultraviolet light through said mask.

54. The method of Claim 53, wherein said printing step further comprises the substep of aligning said mask to an alignment mark on said substrate.

55. The method of Claim 41, wherein said printing step comprises positioning a stencil on or over said substrate, and depositing a layer of said composition in a solvent through said stencil onto said substrate.

56. The method of Claim 41, wherein said printing step comprises inkjet printing said composition in said solvent in said pattern onto said substrate.

57. The method of Claim 41, wherein said printing step comprises screen printing, gravure printing, offset lithography, flexographic printing or laser writing said composition in said solvent in said pattern onto said substrate.

58. The method of Claim 41, wherein said curing step comprises drying said composition and said substrate.

59. The method of Claim 42, wherein said curing step further comprises heating said composition to a temperature of at least about 200 °C. to sinter said passivated semiconductor nanoparticles and said composition.

60. The method of Claim 41, wherein said curing step comprises placing said substrate into a chamber, and evacuating said chamber.

61. The method of Claim 60, wherein said curing step further comprises passing an inert and/or reducing gas into said chamber.

62. The method of Claim 41, wherein said pattern comprises a two-dimensional array of lines having a width of from 100 nm to 100 μm.

63. The method of Claim 62, wherein said lines have an inter-line spacing of from 100 nm to 100 μm.

64. The method of Claim 62, wherein said lines have a length of from 1 μm to 5000 μm.

65. The method of Claim 62, wherein said lines have a thickness of from 0.01 μm to 1000 μm.

66. A method of forming a semiconductor thin film, comprising

a) at least partially curing a thin film composition comprising semiconductor nanoparticles to form a semiconductor thin film lattice,

b) coating the semiconductor thin film lattice with a composition comprising at least one cyclic Group IVA compound of the formula (1):

$$(AH_x)_n, \quad (1)$$

where n is from 3 to 12, each of the n instances of x is independently 1 or 2, and each A in the formula (1) is independently Si or Ge; and/or a second cyclic Group IVA compound of the formula (2):

$$(AH_x)_m(AH_yR_{z-y})_p(ZR'_w)_q, \quad (2)$$

where (m + p + q) is from 3 to 12, each of the m instances of x is independently 0, 1 or 2, each of the p instances of y is independently 0, 1 or 2, each of the p instances of z is independently 0, 1 or 2, each of the p instances of (y + z) is independently 1 or 2, each of the q instances of w is independently 0 or 1, at least one of p and q is at least 1, each A in the formula (2) is independently Si or Ge, Z is selected from the group consisting of B, P and As, and each R in the formula (2) is independently alkyl, aryl, aralkyl, a halogen, $BH_sR"_{2-s}$, $PH_sR"_{2-s}$, $AsH_sR"_{2-s}$ or $AH_tR"_{3-t}$, where s is 0 to 2, t is 0 to 3, R' is R or H, and R" is alkyl, aryl, aralkyl, a halogen, or AH_3; and

c) curing the coated thin film lattice to form the semiconductor thin film.

67. The method of Claim 66, wherein said composition comprises both of said first and second cyclic Group IVA compounds.

68. The method of Claim 66, wherein said semiconductor nanoparticles comprise passivated semiconductor nanoparticles.

69. The method of Claim 66, wherein said semiconductor nanoparticles comprise silicon nanoparticles.

70. The method of Claim 66, wherein said at least partially curing step (a) comprises sintering said semiconductor nanoparticles to form said semiconductor thin film lattice.

71. The method of Claim 70, wherein said sintering comprises heating said semiconductor nanoparticles to a temperature of at least about 200 °C.

72. The method of Claim 71, wherein said temperature is at least about 300 °C.

73. The method of Claim 66, wherein said curing step (c) comprises sintering said coated semiconductor thin film lattice to form said semiconductor thin film.

74. The method of Claim 73, wherein said sintering comprises heating said coated semiconductor thin film lattice to a temperature of at least about 200 °C.

75. The method of Claim 74, wherein said temperature is at least about 300 °C.

76. The method of Claim 66, further comprising patterning said semiconductor thin film.

77. The method of Claim 76, wherein said patterning comprises the substeps of depositing a layer of photoresist on said semiconductor thin film, selectively irradiating portions of said photoresist, removing non-irradiated portions of said photoresist, and removing exposed portions of said semiconductor thin film to form a patterned semiconductor thin film.

78. The method of Claim 66, wherein said coating comprises spin coating, dip coating, or spray coating said composition on said semiconductor thin film lattice.

79. A method of forming a semiconductor thin film, comprising

a) at least partially curing a thin film composition comprising at least one cyclic Group IVA compound of the formula (1):

$$(AH_x)_n, \quad (1)$$

where n is from 3 to 12, each of the n instances of x is independently 1 or 2, and each A in the formula (1) is independently Si or Ge; and/or a second cyclic Group IVA compound of the formula (2):

$$(AH_x)_m(AH_yR_{z-y})_p(ZR'_w)_q, \quad (2)$$

where (m + p + q) is from 3 to 12, each of the m instances of x is independently 0, 1 or 2, each of the p instances of y is independently 0, 1 or 2, each of the p instances of z is independently 0, 1 or 2, each of the p instances of (y + z) is independently 1 or 2, each of the q instances of w is independently 0 or 1, at least one of p and q is at least 1, each A in the formula (2) is independently Si or Ge, Z is selected from the group consisting of B, P and As, and each R in the formula (2) is independently alkyl, aryl, aralkyl, a halogen, $BH_sR"_{2-s}$, $PH_sR"_{2-s}$, $AsH_sR"_{2-s}$ or $AH_tR"_{3-t}$, where s is 0 to 2, t is 0 to 3, R' is R or H, and R" is alkyl, aryl, aralkyl, a halogen, or AH_3;

b) coating the at least partially cured thin film composition with an ink comprising semiconductor nanoparticles; and

c) curing the coated, at least partially cured thin film composition to form the semiconductor thin film.

80. The method of Claim 79, wherein said composition comprises both of said first and second cyclic Group IVA compounds.

81. The method of Claim 79, wherein said semiconductor nanoparticles comprise silicon nanoparticles.

82. The method of Claim 79, wherein said at least partially curing step (a) comprises oligomerizing and/or polymerizing said cyclic Group IVA compound(s).

83. The method of Claim 82, wherein said oligomerizing and/or polymerizing comprises (i) heating said cyclic Group IVA compound(s) to a temperature of at least about 100 °C., (ii) irradiating said cyclic Group IVA compound(s), or (iii) both (i) and (ii).

84. The method of Claim 79, wherein said curing step (c) comprises sintering said coated, at least partially cured thin film composition to form said semiconductor thin film.

85. The method of Claim 84, wherein said sintering comprises heating said coated, at least partially cured thin film composition to a temperature of at least about 300 °C.

86. The method of Claim 79, further comprising patterning said semiconductor thin film.

87. A semiconducting thin film structure comprising a pattern of semiconducting material on a substrate, said semiconducting material comprising a sintered mixture of passivated semiconductor nanoparticles in a hydrogenated, at least partially amorphous Group IVA element, said Group IVA element comprising at least one of silicon and germanium, said semiconducting material having improved conductivity, density, adhesion and/or carrier mobility relative to an otherwise identical structure made by an identical process, but without either the passivated semiconductor nanoparticles or the hydrogenated, at least partially amorphous Group IVA element.

88. The thin film structure of Claim 87, wherein said semiconductor nanoparticles comprise silicon nanoparticles.

89. The thin film structure of Claim 87, wherein said hydrogenated, at least partially amorphous Group IVA element comprises amorphous silicon.

90. The thin film structure of Claim 87, wherein said hydrogenated, at least partially amorphous Group IVA element further comprises a covalently-bonded dopant element selected from the group consisting of B, P and As.

91. The thin film structure of Claim 87, wherein said pattern comprises a two-dimensional array of lines having a width of from 100 nm to 100 μm.

92. The thin film structure of Claim 91, wherein said lines have an inter-line spacing of from 100 nm to 100 μm.

93. The thin film structure of Claim 91, wherein said lines have a length of from 1 μm to 5000 μm.

94. The thin film structure of Claim 91, wherein at least a subset of said lines have a length of from 2 μm to 1000 μm.

95. The thin film structure of Claim 91, wherein said lines have a thickness of from 0.01 μm to 1000 μm.